Hagit Attiya

Title: Fences and RMRs Required for Synchronization

Abstract: Compiler optimizations that execute memory accesses out of (program) order often lead to incorrect execution of concurrent programs. These re-orderings are prohibited by inserting costly fence (memory barrier) instructions. The inherent Fence Complexity is a good estimate of an algorithm's time complexity, as is its RMR complexity: the number of Remote Memory References the algorithm must issue.

We show that ensuring the correctness of objects supporting strongly non-commutative operations (e.g., stacks, sets, queues, and locks), requires to insert at least one read-after-write (RAW) fence. When write instructions are executed in order, as in the Total Store Order (TSO) model, it is possible to implement a lock (and other objects) using only one RAW fence and an optimal O(n log n) RMR complexity. However, when store instructions may be re-ordered, as in the Partial Store Order (PSO) model, there is an inherent tradeoff between fence and RMR complexities.

We will also describe other results related to the fence complexity of transactional memory.

Biography: Hagit Attiya is a professor at the department of Computer Science at the Technion, Israel Institute of Technology, and holds the Harry W. Labov and Charlotte Ullman Labov Academic Chair. Her research interests are distributed and concurrent computing. She is the editor-in-chief of Springer's journal Distributed Computing and a fellow of the ACM. She received the B.Sc. degree in Mathematics and Computer Science from the Hebrew University of Jerusalem, in 1981, the M.Sc. and Ph.D. degrees in Computer Science from the Hebrew University of Jerusalem, in 1983 and 1987, respectively. Before joining the Technion, she has been a post-doctoral research associate at the Laboratory for Computer Science at M.I.T.